Examples of Optoelectronic Integrated Circuits

In this chapter the full variety of receiver OEICs in digital and analog techniques will be introduced. Examples of optical receivers range from low-power synchronous digital circuits for massively parallel optical interconnects and three-dimensional optical memories to Gb/s fiber receivers. Low-offset analog OEICs for two-dimensional optical memory systems such as CD-ROM and digital-versatile-disk (DVD) will be described as well as image sensors. Hybrid integrated laser drivers are included as examples of optical emitters.

12.1 Digital CMOS Circuits

In this section, the properties of digital CMOS OEICs are described because of their potential application in massively parallel optical interconnects and volume holographic optical memories. Synchronous circuits are appropriate for such purposes. Furthermore, an asynchronous photoreceiver for application in the testing of digital CMOS circuits on the wafer level deserves to be described here.

12.1.1 Synchronous Circuits

For the application in massively parallel optical interconnects between VLSI chips, a novel monolithic optoelectronic receiver system was presented in a standard 0.7 µm N-well CMOS technology [593]. The circuit, which requires two clock signals, reset (RST) and store (STORE), and therefore is a synchronous circuit, is shown in Fig. 12.1.

The heart of the synchronous receiver is a CMOS bistable flip-flop, which acts as a sense-amplifier. The flip-flop is formed by two CMOS inverters, M2/M4 and M3/M5. The input of each inverter is connected to the output of the other inverter. In such a way, a dual state can be stored. In order to use the flip-flop as a light receiver, two photodiodes were added to the drains of the P-channel transistors M2 and M3. In fact, the diodes were not separated
Fig. 12.1. CMOS synchronous photoreceiver circuit [593]

Fig. 12.2. Cross section of MOS transistors with enlarged drain areas as photodiodes [593]

from the transistors. The diodes were obtained by extending the drains to an area of $15 \times 15 \mu m^2$. The P$^+$ drain island and the N well, therefore, form the photodiode (Fig. 12.2).

The timing of the synchronous receiver is shown in Fig. 12.3. Before the flip-flop can receive, i.e., store, a new bit, a reset signal has to be applied to M6. During this reset signal, the flip-flop is deactivated by a low voltage level at the gate of M7 and by a high voltage level at the gate of M1. M6 is conducting during reset and forces the nodes Q and NQ to the same potential. After the reset phase, M6 is switched off and light can fall into one of the diodes, let us say into D1. Electron–hole pairs are generated at the P$^+$N junction between the drain of M2 and the N well. The N well is biased at VDD = 5 V. The potential of the drain can be assumed to be at a floating level of approximately VDD/2. The P$^+$N photodiode is biased in the reverse direction,
and the photogenerated carriers are separated in the electric field region of the PN junction effectively. The photogenerated electrons drift into the N well and the photogenerated holes drift into the P$^+$ region. There is also a slower contribution of diffusing minority carriers to the photocurrent, because the light penetrates also in deeper field-free regions of the N well. As a consequence of the photocurrents, the potential of node Q becomes more positive than that of node NQ. When the supply voltages are applied to the flip-flop via M1 and M7, the sense-amplifier flip-flop begins to work. A more positive input signal of the inverter M3/M5 results in a more negative output signal at node NQ, which causes a higher output signal of the inverter M2/M4 at node Q. This amplifying ring process continues until digital levels, i.e., VDD, and ground levels are obtained at the two output nodes Q and NQ of the flip-flop, respectively. It was reported that this final stable state was reached after approximately 3 ns from the beginning of the light incidence [593].

A minimum light input energy of 176 fJ, which corresponds to an optical power of 59 µW within a time interval of 3 ns, was needed for an optical wavelength of 830 nm in order to obtain a correct decision of the sense-amplifier flip-flop. This minimum light energy causes a voltage change of 264 mV at node Q [593]. This voltage change is amplified by the flip-flop to a digital level. With the PMOS version described above, a bit rate of 120 Mb s$^{-1}$ was obtained. In the NMOS version, i.e., using the N$^+$-drain to P-substrate diodes of the transistors M4 and M5 as photodiodes (see Figs. 12.1 and 12.2), a maximum bit rate of 180 Mb s$^{-1}$ was reported. This higher speed of the NMOS version of the synchronous receiver can be explained by the faster diffusion of electrons in the P substrate. The PMOS version is slower because holes

Fig. 12.3. Timing diagram of a synchronous CMOS photoreceiver [593]
are the minority carriers in the N well, and holes are diffusing slower than electrons due to the lower hole mobility.

For massively parallel optical interconnects, it is necessary to minimize the die area of the receivers. The receiver circuit shown in Fig. 12.1 occupied an area of $55 \times 24 \mu m^2$ without the output buffers. The synchronous receiver with the sense-amplifier flip-flop is especially interesting for the application in massively parallel optical interconnects due to its very small area consumption.

The function of this receiver is called synchronous because the clock signals, reset and store are needed. These signals have to be transmitted in additional optical fibers, for which asynchronous receivers are needed, or have to be supplied electrically.

In the following, another application of sense-amplifier flip-flops, where the reset and store signals are readily available, will be described. Sense-amplifier flip-flops can readily be used for the read process of page-oriented optical memories (POMs), such as volume holographic storage systems [594]. Such optical memories need highly parallel read circuits. A small size of each detector and each amplifier is, therefore, essential. The clock signals for reset and store (or latch) of the sense-amplifier flip-flop are readily available in optical memories, and these signals do not have to be extracted for this application. The POMs offer the potential for high capacity, random access times from 10 to 100 $\mu$s, and page sizes up to 1 Mb, yielding data transfer rates of $10$–$100$ Gb s$^{-1}$. Maximum output data rates of 250 Mb s$^{-1}$ for CCD arrays [171] are insufficient for POM systems. Pixel circuits, like that in Fig. 12.4 with sense-amplifier flip-flops, combine a large speed, a high gain, and a small size. They can be embedded in each pixel yielding active receivers in a highly parallel arrangement.

![Fig. 12.4. Photoreceiver circuit for smart photodetector array [595]](image-url)
The circuit of a pixel in a photodetector array for a page-oriented optical memory (Fig. 12.4) combines two flip-flops (latches) in order to achieve a high gain.

The operation of the circuit is controlled by reset \( \overline{\text{RST}} \) and latch \( \overline{\text{LAT}} \). The P latch with transistors P1 and P2 is isolated from the N latch with N1 and N2 via P3 and P4 for \( \overline{\text{LAT}} = 1 \). The pull-down devices N3 and N4 are conducting, and the N latch is reset for \( \overline{\text{LAT}} = 1 \). Next \( \overline{\text{RST}} \) is set to 0. During this reset, the photosensitive inputs A and B are shorted through P5 and \( V_A = V_B = V_{\text{RST}} \approx V_{DD} + V_{\text{Th,PMOS}} \). When \( \overline{\text{RST}} \) is taken high again, parasitic capacitances hold nodes A and B at \( V_{\text{RST}} \) putting the P latch in a metastable state. A photocurrent \( I_{\text{ph}} \) at one of the differential inputs causes the corresponding input voltage to drop. Positive feedback in the P latch increases the differential voltage. When \( \overline{\text{LAT}} \) is changed to 0, this differential voltage is amplified by the N latch and the signal is acquired at Q and \( \overline{Q} \). P1 and P2 should be small in size for a high sensitivity to small photocurrents. The static power consumption of the circuit in Fig. 12.4 is determined by leakage currents. The dynamic power consumption mainly depends on the capacitance of the photodiode. In [595], the N-well to P-substrate photodiode in a 0.35 \( \mu \)m CMOS process was used with a photosensitive N-well area of 50 \( \times \) 50 \( \mu \)m\(^2\). The capacitance of this photodiode was approximately 1 pF. The size of the photoreceiver circuit in Fig. 12.4 without the photodiodes was 20 \( \times \) 22 \( \mu \)m\(^2\). An optical power of 2.5 \( \mu \)W for \( \lambda = 839 \text{nm} \) was necessary to toggle the receiver. With an assumed photodiode responsivity of 0.3 A W\(^{-1}\), a switching energy of 150 fJ was estimated [595]. A single-pixel data rate of 245 Mb s\(^{-1}\) was determined for the circuit in Fig. 12.4. With the circuitry necessary for error correction, a maximum pixel number of approximately 26,700 per 0.35 \( \mu \)m CMOS chip was projected in [595]. The bit rate per chip for corrected data was estimated to be 102 Gb s\(^{-1}\) stemming from the high parallelism.

### 12.1.2 Asynchronous Circuits

Compact and fast photoreceivers with on-chip photodiodes in standard CMOS technology have been developed as optical inputs for testing of digital circuits [596]. Novel CMOS circuits work at increased speed and they cannot be tested on the wafer level at their working speed with conventional electric needle contacts. In order to overcome this limitation, optical inputs can be used. The light is coupled into photodiodes on the chips via optical fibers being adjusted on a wafer prober (Fig. 12.5). The outputs of the chip having lower frequency were contacted with electric needles or capacitively with a special probe sensor. The output signals are checked for correctness by the comparator in a test equipment (Fig. 12.5).

In a 1.5 \( \mu \)m CMOS technology, an input frequency of 250 MHz was obtained for an optical wavelength of 635 nm with an optical receiver requiring a die area of only 70 \( \times \) 70 \( \mu \)m\(^2\). Maximum input frequencies of 243 and 187 MHz
were reported for the wavelengths of 685 and 787 nm, respectively. The N⁺-source/drain to P-substrate diode in the N-well CMOS process was used for the photodiodes with an area of \(20 \times 20 \mu\text{m}^2\). The speed of the circuit test on the wafer was increased several times compared with the conventional electrical input technique using this optical input technique. This performance could be obtained with a current comparator circuit with a statically supplied reference photodiode. The circuit diagram of this photoreceiver is shown in Fig. 12.6.

The transistors M1, M2 and M3, M4, respectively, form current mirrors, which amplify the photocurrents of the signal and reference photodiodes. The transient response has its optimum for a width ratio \(W_2/W_1\) of 2–2.5 \[596\]. The amplified photocurrents are compared to each other by the transistors M2 and M4. The advantage of this configuration is its good sensitivity to small differences in the photocurrents due to the high impedance node N3. Because of the high drain resistances, a small difference in the currents results in a large voltage change. The advantage of this photoreceiver clearly is that the photocurrent of the N⁺P signal photodiode does not have to drop much to obtain a logical zero at the output node N3 of the current comparator, when the light is switched off for a short period, i.e., a large contribution of the slow diffusion current to the photocurrent is possible. It has to be mentioned,
however, that large photocurrents and large optical powers are necessary to obtain fast current mirror amplifiers. The optical power used for chip testing was of the order of 1 mW [596]. Another advantage of this current comparator circuit is its robustness for the application in automatic chip testers. Compared to the synchronous receiver shown in Fig. 12.1, the current comparator circuit shown in Fig. 12.6 works asynchronously and, therefore, does not need overhead circuitry for timing. The speed of the current comparator circuit in a 1.5 μm CMOS technology is comparable to the speed of the synchronous receiver in a 0.7 μm CMOS technology for the optical wavelength of 787 nm. The speed of the current comparator circuit, therefore, can be improved considerably using a technology with a smaller gate length. The signal photodiode feeding an N-channel current mirror and the reference photodiode feeding the P-channel current mirror probably would allow a further increase in the input frequency.

12.2 Digital BiCMOS Circuits

The principle of a current comparator circuit shown in Fig. 12.6 for a CMOS photoreceiver was also applied to a BiCMOS photoreceiver for the high speed testing of frequency dividers on the wafer level [597]. Figure 12.7 shows the BiCMOS version of a current comparator. In the 1.2 μm BiCMOS process,
fast NPN transistors were available, which preferably were used in the signal current mirror. The slower P-channel current mirrors are kept for the reference path.

The circuit shown in Fig. 12.7 was used for a high speed test of a BiCMOS frequency divider on the wafer level. N$^+$ to P-substrate and P$^+$ to N-well photodiodes with areas of 20 × 20 µm$^2$ were used. A frequency of 800 MHz was successfully fed into the BiCMOS frequency divider optically with a wavelength of 635 nm via a single-mode fiber. The optical output power of the commercially available semiconductor laser used in [597] was of the order of 1 mW. The area consumption of an optical input was reported to be less than 70 × 70 µm$^2$.

### 12.3 Laser Driver Circuits

A simple two-transistor CMOS driver (Fig. 12.8) based on a current-shunting principle, which provides a low-area, tunable power circuit with a measured small-signal bandwidth of 2 GHz in 0.5 µm CMOS technology, has been implemented in a flip-chip bonded CMOS VCSEL chip [443].

The PMOS transistor is used to supply an adjustable current through the laser, and the NMOS transistor is used to quickly shunt the current into and
out of the VCSEL for digital operation. The multimode VCSELs could be operated at 1.25 Gb s$^{-1}$ from below the laser threshold in this digital operation. In this case, the eye pattern indicated a turn-on delay of the lasers of about 180 ps. For a bit error rate of less than $10^{-11}$ at 1.25 Gb s$^{-1}$, the total power consumption of one driver and laser was about 17.5 mW at an optical power of $-6.9$ dB m. The NMOS transistor used as a small signal modulator, reducing the laser current only by a small amount and especially not below the threshold current, allowed to verify a bandwidth of the order of 2 GHz. This low-power high-speed operation demonstrates the utility and potential of the flip-chip bonding technique for optical interconnect technology.

Another hybrid CMOS-VCSEL transmitter has been introduced [598]. An array of eight GaAs–AlAs lasers with an InGaAs triple-quantum-well active region was wire-bonded to driver circuits in a 1.0 $\mu$m CMOS technology. The threshold current $I_{th}$ of the lasers was 2.7 mA, and the peak optical output power exceeded 1 mW without heat sinking. Typical turn-on voltages $V_{ld}(I_{th})$ were $(3 \pm 0.5)$ V. The driver circuit is shown in Fig. 12.9.
Since the laser array had one common cathode, only the lasers’ anode terminals are independent, and the modulation current $I_m$ is controlled by the PMOS transistor $M_1$. The PMOS transistor $M_4$ regulates the laser bias current, which has to be somewhat larger than $I_{th}$ in order to allow fast laser modulation. By minimizing stored charge in the current steering transistors, fast rise and fall times with low jitter and skew can be achieved. The choice of the width of $M_1$, however, is a trade-off between low parasitic capacitance for small device width and a reduced output impedance for a large width. A device width of 500 $\mu$m has been chosen as a good compromise for $I_m = 15$–25 mA in [598].

The NMOS devices $M_5$ and $M_6$ together with the inverter between their gates perform a single-ended to differential conversion. The NMOS device $M_3$ controls the modulation current $I_m$. The PMOS transistor $M_2$ serves as a current mirror reference in the “1” state and is a self-biased inverter in the “0” state. In such a way, $U_{gs}$ of $M_1$ is not zero but approximately equal to the threshold voltage in the “0” state, when the laser is off and a high modulation speed can be obtained. In the “1” state, $I_2$ is mirrored (amplified by a certain factor) through $M_2$ to $M_1$ and into the laser. With a 50 $\Omega$ resistor load instead of the laser and with $I_m = 25$ mA, the rise and fall times were about 0.5 ns, and the eye pattern was wide open at 622 Mb s$^{-1}$. When a chip with eight CMOS drivers was incorporated into one package with a VCSEL array flip-chip mounted onto a BeO substrate, the bond-wire inductances somewhat degenerated the slew rate [598]. A data rate of 622 Mb s$^{-1}$ with a bit error rate of less than $10^{-9}$, however, still has been obtained.

The cell size of one driver circuit with output pads was $175 \times 300 \mu m^2$. The average power dissipation of one channel was 137 mW for an optical output power of 1 mW with $I_m = 20$ mA, where the laser consumed 75 mW (55%), $M_1$ dissipated 45 mW (33%), and its driver used 17 mW (12%). For an array with many CMOS-VCSEL channels, this large power dissipation generates too much heat, and better designs are necessary.

A laser driver circuit consisting of two N-channel MOS transistors (see Fig. 12.10) is advantageous compared with the shunt driver circuit in Fig. 12.8 with respect to power consumption. Here, $M_2$ is used to bias the laser above threshold (“0”) and $M_1$ increases the laser current in order to obtain a high optical output power (“1”). Here, the current flowing continuously is lower than in the shunt driver circuit shown in Fig. 12.8. The circuit in Fig. 12.10 was implemented in [599] to modulate flip-chip bonded InGaAs quantum well VCSELs with an $I_{th}$ of 6.4 mA.

The N-channel MOSFETs had a gate length of 0.8 $\mu$m and a gate width of 30 $\mu$m. With $V_{mod}$ between 3.2 and 5 V, the optical output power could be controlled between 0.05 and 1.3 mW, when $V_{DD} = 8.5$ V had been chosen. A possible modulation rate of 2 Gb s$^{-1}$ for the circuit in Fig. 12.10 has been estimated [599].
12.4 Analog Circuits

In this section, a bipolar amplifier circuit, for an optical flame detection system, with a very high transimpedance of $1.1 \times 10^9 \text{VA}^{-1}$ will be described. Another bipolar amplifier for audio CD systems is also described because of a so-called T-type feedback circuitry.

Two pixel circuits of a-Si:H CMOS image sensors with reduced cross-talk and a very high dynamic sensitivity range, respectively, and a fingerprint detector using lateral bipolar transistors will follow. Then CMOS and BiCMOS circuits for optical storage systems are described.

Finally, fiber receiver circuits in bipolar SiGe, NMOS, BiCMOS, and CMOS technology are explained. A comparison of the performance of optical silicon receiver circuitry compactly represents the state of the art.

12.4.1 Bipolar Circuits

The detector of a UV-sensitive OEIC [47] was already described in Sect. 3.3. The electronic circuit of the UV sensor system for flame detection where the photocurrent was only 20 pA to 1 nA will be explained here.

Because of the small photocurrents, a large amplification with a large transimpedance of $10^9 \text{VA}^{-1}$ was necessary in order to obtain signal voltages of up to 1 V. Fortunately, the system did not require accurate control of the gain and, therefore, the current amplification factors of the NPN and PNP transistors of the complementary bipolar process could be fully exploited without a feedback circuitry. The circuit diagram of the bipolar amplifier is shown in Fig. 12.11.

The transistors $Q_{13}$ and $Q_{15}$ both in common base configuration together with their current sources $Q_{12}$ and $Q_{14}$, respectively, provide a low-impedance input for the photocurrent ($R_{\text{in}} = 1/g_{m,13}$). The UV photodiode is biased at zero volts. The anodic UV photocurrent $I_{\text{UV}}$ (compare Fig. 3.6) flows into the emitter of $Q_{13}$ and is injected into the base of $Q_{16}$. Transistor $Q_{16}$ amplifies the photocurrent by its current gain factor $\beta_{16}$. This amplified current forms the base current of $Q_{18}$. At the collector of $Q_{18}$, the photocurrent is amplified

Fig. 12.10. Laser driver circuit with two NMOS transistors [599]
by the value of the product $\beta_{16} \times \beta_{18}$. The collector current of $Q_{18}$ is mirrored into $Q_{24}$ by $Q_{21}$ and finally transformed into a voltage by $R_3$.

The infrared-dependent cathodic current $I_{UV} + I_{IR}$ (see Sect. 3.3) is shunted to $V_{CC}$ by $Q_{14}$. The transistors $Q_{10}$ and $Q_{11}$ supply a reference bias current $I_B$ to $Q_{20}$, which is the input of the second branch of the differential amplifier with $Q_{16}$, $Q_{18}$, $Q_{19}$, and $Q_{20}$. A reference current amplified by $\beta_{19}$ and $\beta_{20}$ is mirrored via $Q_{22}$ and $Q_{23}$ to $R_2$. The voltage $V_o$ across the output terminals of the circuit is, therefore, given by

$$V_o = \beta_{16}\beta_{18}KR_3(I_{UV} + I_B) - \beta_{19}\beta_{20}KR_2I_B. \quad (12.1)$$

When perfect device matching ($Q_{16} = Q_{20}$, $Q_{18} = Q_{19}$, and $R_2 = R_3$) can be assumed, the output voltage $V_o$ does not depend on the bias current $I_B$:

$$V_o = \beta_{16}\beta_{18}KR_3I_{UV}.$$

For the complementary bipolar process, $\beta$ is approximately 140. $R_3$ was designed to be 28 k$\Omega$, and the mirror factor $K$ was 2. This resulted in a transimpedance of $1.1 \times 10^9$ V$A^{-1}$.

Although the output voltage is independent of $I_B$, $I_B$ has to be very well controlled for correct operation, and it has to be very small, because of the large transimpedance value. The bias section $Q_1$ to $Q_9$ replicates the gain stage ($Q_4$ corresponds to $Q_{18}$, $Q_5$ corresponds to $Q_{16}$, and $R_1 = R_3$) and feeds back the proper bias current via $Q_6$, $Q_{10}$, and $Q_{12}$. $I_B$ can be adjusted accurately in the nA range with the reference voltage $V_B$. For $V_B$ ranging from 0 to 3.5 V, $I_B$ is adjustable between 15 and 0 nA. The compensation capacitor $C = 12$ pF is needed for the stability of the feedback loop.

The response time of the sensor of less than 100 ms was determined by the capacitance of the UV photodiode and the small photocurrents. The input-equivalent noise was smaller than 3.7 pA per $\sqrt{\text{Hz}}$ at 1 Hz. The power consumption of the UV-OEIC was 4 mW at 5 V. The total chip area was 4 mm$^2$ of which the UV photodiode occupied 1 mm$^2$. 

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**Fig. 12.11.** Circuit diagram of a UV sensitive OEIC [47]
After this example of an open loop very-high-gain amplifier, an amplifier with a T-type feedback network will be explained. Such a bipolar preamplifier OEIC for compact disk (CD) systems was described in [600]. The amplifier provides a high transimpedance gain, i.e., a low photocurrent is converted to a large voltage, and a relatively large bandwidth. In order to achieve these properties, the feedback via the T-type network shown in Fig. 12.12 is applied.

The T-type network consists of the resistors $R_{F1}$, $R_{F2}$, and $R_{F3}$, whereby the values of $R_{F1}$ and $R_{F2}$ were chosen to be equal in [600]. The T-type network is an appropriate measure to simulate a high resistance $R_F$ with low resistor values. The effective value of $R_F$ is

$$R_F = \frac{R_{F1}R_{F2} + R_{F1}R_{F3} + R_{F2}R_{F3}}{R_{F3}}$$

and the output voltage $V_o$ is obtained

$$V_o = -I_{ph}R_F.$$ 

In such a way, it is possible to construct high-gain amplifiers without a high-resistivity polysilicon process module. Emitter polysilicon or gate polysilicon in a (Bi)CMOS process is sufficient. The T-type feedback can also be considered as a means to avoid large RC time constants of large resistance values, requiring a large polysilicon area with a large parasitic capacitance. Effective resistance values of 82 kΩ for a maximum photocurrent of 1.2 µA and of 328 kΩ for a photocurrent of 0.3 µA were realized in [600], whereby the true resistors had much lower values and the die area could be kept low at 400 × 350 µm². It should be mentioned, however, that the input offset voltage of the operational amplifier is also amplified [601].

The circuit is shown in Fig. 12.13. Only NPN transistors are used in the OEIC for a compact disk (CD) system in order to achieve a large bandwidth. The transit frequency of NPN transistors was 1.5 GHz. The operational amplifier has the voltage followers Q3 and Q4 in front of the common-emitter
difference amplifier stage Q1/Q2 to obtain a low input current, whereby a large offset voltage due to the voltage drop across the T-type network caused by the base current of Q2 can be avoided.

The transistors Q2 and Q5 form a cascode stage to avoid a large Miller capacitance of Q2. High performance PNP transistors were not available, and instead of a PNP current mirror load, the resistor $R_C$ is used. Another voltage follower is used in order to obtain a low output impedance and isolate the collector of Q5 from the load capacitance. The low-frequency open-loop gain was estimated to be $A_0 = 0.5g_m R_C = 40$. A compensation network was reported to be necessary; however, it was not described in [600]. The photodiodes used in the CD-OEIC also were not described.

The complete CD-OEIC contained fast channels with a bandwidth of 16 MHz for a maximum photocurrent of 1.2 $\mu$A and slower channels for a photocurrent of 0.3 $\mu$A. For the fast channels, rise and fall times of 22 ns with a settling time to 0.1% of 200 ns were reported. The systematic offset voltage due to the base current of Q4 was smaller than 4 mV. The power consumption for one fast channel was 9.8 mW at 5 V.

### 12.4.2 CMOS Imagers

In Sect. 3.5.15, the concept of Thin Film on ASIC (TFA) was described. As an alternative to a self-structuring technology for the a-Si photodetectors in image sensors, an electronic circuit within each pixel was presented which reduces cross talk between neighboring pixels [264]. The TFA sensor overcoming the coupling effect of neighboring photodetectors in an unstructured a-Si:H film by electronic means was called AIDA (Analog Image Detector Array). A circuit inside each pixel (in c-Si) provides here a constant rear electrode potential for
the photodetectors, thereby, eliminating lateral currents between neighboring photodetectors in the a-Si:H film. The photodetectors are used in a constant voltage mode. The circuit diagram of a pixel is given in Fig. 12.14. Each pixel consists of an a-Si:H photodetector, eight MOSFETs, and one integration capacitance $C_{\text{int}}$. $C_{\text{int}}$ is discharged by the photocurrent. The inverter M2, M3, and the source follower feedback M1 keep the cathode voltage of the detector constant. M4 limits the power consumption of the inverter. M5 restricts the minimum voltage across the integration capacitance to 1.2 V in order to always keep the constant voltage circuit working. The integrated voltage on $C_{\text{int}}$ is read out via M7 in source follower configuration and via the switch M8. The reset operation is performed as M6 recharges $C_{\text{int}}$ after readout. The effective integration time of the pixel is the time period between two reset pulses, because readout is nondestructive and is performed at the end of the integration period.

The integration time may be varied according to the brightness of the scene. By this means, the sensitivity is controlled for all pixels globally. The AIDA sensor consists of $128 \times 128$ pixels with a size of $25 \times 25 \mu m^2$ each. The dynamic range of the sensor amounts to 60 dB for an integration time of 20 ms. The dynamic range can be extended significantly by means of the sensitivity control. The sensor was tested for illumination levels as high as 80,000 Lux. No blooming effects or image lag were observed [264].

For applications of an image sensor in a vehicle guidance system, for instance, which requires a very high degree of safety, the global sensitivity

![Fig. 12.14. Circuit diagram of a pixel in AIDA for operating the photodiode in a constant voltage mode [264]](image-url)
control is not appropriate. A number of pixels with excessive illumination may be saturated, whereas only slightly illuminated pixels may generate signal voltages below the noise and dark current levels. As pixels with logarithmic output characteristics exhibited a seriously increased sensitivity to temperature changes and fixed pattern noise, a Locally Adaptive Sensor in TFA-technology (TFA-LAS) was suggested [264]. The TFA-LAS allows to control the integration time and, therefore, the sensitivity of each pixel individually [602]. Figure 12.15 gives the complete pixel circuitry realized in the c-Si below each a-Si:H pixel photodetector.

The photocurrent is integrated into the MOS capacitance $C_{\text{int}}$ while the rear electrode of the photodiode (cathode) is kept at a constant potential (compare Fig. 12.14). The integration time value is calculated externally for each illumination period and programed into the pixel as an analog voltage $V_{\text{prog}}$, which is stored on the capacitor $C_{\text{prog}}$. $V_{\text{prog}}$, standing at $D_{\text{inout}}$, is switched via $N_{13}$ to $C_{\text{prog}}$ for this purpose. This voltage on $C_{\text{prog}}$ is compared to a linear voltage ramp generated by the peripheral electronics during the integration phase. The comparator consisting of the transistors $N_{1}$–$N_{5}$ and $P_{6}$–$P_{8}$ starts the integration as soon as the voltage ramp rises above $V_{\text{prog}}$ and stops it at the falling edge of the ramp. A standard 0.7 µm CMOS ASIC technology implementing the TFA-LAS pixel schematic of Fig. 12.15 enabled a dynamic illumination range of more than 100 dB throughout the complete pixel array at any time. This corresponds to the outstanding dynamic range of c-Si PIN detectors, which is over 100 dB at an illumination intensity of 1,000 Lux. For the TFA-LAS, the voltage range for the pixel signal amounts to 54 dB. The remaining dynamic range of 46 dB is included in the integration time and, therefore, in the programing voltage. The combination of both signal

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**Fig. 12.15.** Pixel circuit diagram of a locally adaptive image sensor [264]
and programing voltage, thus, gives the information on the illumination level of a specific pixel. The TFA-LAS consisted of $64 \times 64$ pixels with a size of $40 \times 50 \mu m^2$ each.

Another interesting CMOS image sensor in bulk silicon should be mentioned here. It combines a lateral bipolar phototransistor array and a current comparator for digitizing the image [129]. The lateral bipolar phototransistor described in Sect. 3.5.6, Fig. 3.64 was used as a photodetector in a fingerprint detection chip fabricated in standard CMOS technology. The fingerprint detection chip contained an $64 \times 64$ array of the lateral phototransistors.

The phototransistors in the array were scanned by connecting one at a time to a current comparator using MOS transistors as selection switches. The circuit of the current comparator is shown in Fig. 12.16.

A threshold must be established so that pixel current values may be compared to give a black/white image. The most convenient point to place the threshold is the average of all pixel currents to obtain a global average. It may also be advantageous to select only $m$ pixels from the entire array to give a local average from a sub-array. The average of the pixel currents is then obtained by dividing the measured current by $m$. In the fingerprint detection system, for instance, four rows of the $64 \times 64$ array were used and a 256:1 current mirror was used to give the average pixel current. The current mirror gate voltage is stored on a 10 pF capacitor. From this capacitor, the reference voltage $V_{\text{ref}}$ is derived setting the reference current for the current comparator. During the following 4,096 clock cycles, all pixels are selected one at a time and their photocurrents are digitized to “1” or “0” by the current comparator. During each clock cycle, one selection MOS switch is activated and the pixel current is pulled through the PMOS current mirror M1 and M2 (Fig. 12.16). If this pixel current is greater than the average current, which was set up through M3 and M4, $V_{\text{out}}$ goes high; otherwise $V_{\text{out}}$ goes low. The transistors M5–M12 compose a noninverting Schmitt trigger, which imposes a hysteresis and, in turn, a stable digitization.
The field of application of such an image detection system is not limited to a fingerprint detection system, of course. Other types of pictures can also be digitized.

### 12.4.3 CMOS Circuits for Optical Storage Systems

Compact disk (CD), CD-ROM, and Digital-Video-Disk (DVD) are optical storage (OS) systems with a storage capacity of the order of 1–10 GByte. The stored information is read with a focused laser beam. Depending on the stored state of 0 or 1, more or less light intensity is reflected into the read circuit, which we will call OS-OEIC. Special arrangements of 6–8 photodiodes are implemented in OS-OEICs to obtain the signals for tracking and for focusing in addition to the RF signal, which contains the stored information (see Fig. 12.17). In contrast to the name digital-video-disc-system, the DVD-OEIC is a purely analog front-end circuit, which is a key-device for the whole DVD-system. OS-OEICs for CD and CD-ROM are also analog circuits. The data rate and, therefore, the speed of the optical storage system are determined by the OS-OEIC.

In OS systems, accordingly, the demand for fast OEICs is steadily increasing, especially in the red spectral range ($\lambda \approx 635–650\text{nm}$). The integration of both the optical devices and the electronic circuits on the same chip leads to a smaller die area, to lower manufacturing costs and to faster systems. Furthermore, the reliability and the immunity against electromagnetic interference of OEICs are enhanced when compared with a two-package solution with a photodiode package and an amplifier package. In comparison to a two-chip solution with a photodetector chip being wire-bonded to an amplifier chip in one package, the die area consumption of a monolithic OS-OEIC is smaller, because the area of a photodiode in an OS system is smaller than the area of a bondpad.

![Diagram of OEIC for compact disc, CD-ROM, and DVD applications](image-url)
For fast OS systems, integrated PN photodiodes are not sufficient, because only a bandwidth of 10–15 MHz is achievable [68, 70]. Although a $-3$ dB bandwidth of 32 MHz can be derived from the frequency response of a $P^+$ to N-substrate photodiode shown in Fig. 3.15, the photocurrent already begins to decrease at a frequency of 2 MHz due to the slow diffusion of photogenerated carriers. Hence, PIN photodiodes are required. It was shown that for the integration of a PIN photodiode in a standard twin-well CMOS process (1 $\mu$m), which uses epitaxial wafers, little modification is necessary. Compared to the published approaches in [38] and [59] with standard-buried-collector (SBC) based bipolar OEICs, less additional process complexity is required [89] as was already pointed out in Sects. 3.3.2 and 3.5.3. The cross section of the CMOS-OEIC was already shown in Fig. 3.36.

To obtain fast integrated PIN photodiodes, the standard doping concentration of the epitaxial layer of $1 \times 10^{15} \text{ cm}^{-3}$ has to be reduced to approximately $5 \times 10^{13} \text{ cm}^{-3}$ [89]. This reduction of the doping level does not influence the electrical parameters of the CMOS devices, since the MOSFETs are placed in wells and, therefore, the model parameters for circuit simulation did not have to be modified for the design of the OEICs [95]. ESD (electrostatic discharge) and latch-up immunity could be obtained by appropriate layouts.

OS-OEICs have to fulfill a stringent requirement concerning the output offset voltage. This requirement implies that only operational amplifiers can be used. Other amplifier types and especially amplifiers without feedback, which could be fast, do not guarantee that the output signals refer to the same reference voltage for a dark detector field within several millivolts.

The PIN photodiodes were integrated together with operational amplifiers in a voltage follower configuration (see Fig. 12.18), since a transimpedance amplifier, which is normally used for small photocurrents, was not advantageous in a digital CMOS process [95]. In order to compare the performance of a monolithically integrated and a wire-bonded circuit, which corresponds to a two-chip solution with photodiode chip and amplifier chip in one package, two test OEICs were developed. In the first case, the PIN photodiode was

![Fig. 12.18. Circuits of monolithic and wire-bonded CMOS DVD OEICs [95]](image-url)
directly connected to the input of the CMOS operational amplifiers, whereas in the second case the PIN photodiode is connected via two bondpads with the input of the CMOS operational amplifier (see Fig. 12.18). This is not really a wire-bonded circuit, but it was possible to demonstrate the benefits of the monolithically integrated circuit [95]. A discrete circuit with an external photodiode has an even poorer performance than the wire-bonded two-chip circuit due to package pin capacitances.

The voltage follower was realized by a two-stage CMOS operational amplifier, which was compensated ($R_C, C_C$) to ground (see Fig. 12.19). This compensation technique was implemented instead of the Miller compensation because of the digital CMOS process. Because of the unavoidable use of the MOS capacitance, a larger voltage drop across the capacitance was necessary in order to avoid the dip in the capacitance/voltage (CV) curve and, therefore, to obtain a practicable size (for the layout) and a value, which was more independent of process deviations within the relatively wide specification limits of the digital CMOS process.

The dimensions of the transistors were chosen to satisfy the zero-systematic-offset condition, which is given by the following equation [604]:

$$\frac{(W/L)_3}{(W/L)_6} = \frac{(W/L)_4}{(W/L)_6} = \frac{1(W/L)_5}{2(W/L)_7}$$

According to circuit simulations, the open loop gain $A_0$ of the operational amplifier was larger than 40 dB for a load of 1 kΩ parallel 10 pF for all operating temperature and transistor parameter combinations. The phase margin was 46°, 58°, and 68° for the “fast” case with the lowest temperature, for the “nominal” case with room temperature, and for the “slow” case with the highest temperature, respectively.
Samples on different N-substrate wafers (doping concentration in the epitaxial layer: approximately $1 \times 10^{15} \text{ cm}^{-3}$ and $5 \times 10^{13} \text{ cm}^{-3}$) were compared. The monolithic test circuit consisted of a PIN photodiode ($\approx 50 \times 50 \mu\text{m}^2$) with an integrated load resistor ($\approx 20 \text{k}\Omega$), which was realized by an N-MOSFET, since no analog high polysilicon resistors were available, followed by the CMOS operational amplifier in a voltage follower configuration (see Fig. 12.18). The voltage follower was loaded with $C_L = 10 \text{pF}$ and $R_L = 1 \text{k}\Omega$ (nominal values) for the measurements. The “wire-bonded” test circuit consisted of the same modules plus two additional bondpads between PIN photodiode and operational amplifier. ESD-protection circuitry was implemented in all the chips to guarantee ESD immunity.

In the following, measured results will be presented. The supply voltage of the OEICs was $5 \text{V}$, $U_{\text{ref}} = 2.5 \text{V}$, and the wavelength of the laser light was $\lambda = 638 \text{nm}$. The laser light was coupled into the photodiodes of the OEICs on the wafer prober via a single-mode fiber. A network analyzer HP8751A was used for the modulation of the laser and for the frequency response measurements of the OEICs.

Figure 12.20 shows a microphotograph of the test circuits. On the left half of the figure, the fully integrated circuit and on the right half the “wire-bonded” circuit are located. The operational amplifiers are located in the upper half of the chips, whereas the integrated resistors are placed in the lower

![Fig. 12.20. Microphotograph of a test chip for the comparison of monolithic and wire-bonded CMOS receiver OEICs. The circuit on the left represents the monolithic OEIC, whereas the circuit on the right representing the wire-bonded OEIC includes two bondpads between photodiode and amplifier in the upper part of the chip][95]
The PIN photodiode with a 50µm wide metal shield and a guard ring around is located in the middle part of the chips with an additional substrate contact, which, however, was not used. The layout was not area-optimized since it was only a test chip.

Furthermore, an 8-channel OEIC for universal focusing and tracking methods of optical storage systems such as DVD was designed [95]. This OEIC consists of 8 channels with PIN photodiodes and voltage followers. Four channels were so-called fast channels for data extraction and focusing and the other four channels were so-called slow channels with a ten times larger sensitivity. The gain of the amplifiers in the fast and slow channels is switchable (high, medium, and low), so that three levels of photocurrent in DVD-ROM and DVD-RAM applications can be detected and amplified. This OEIC was also integrated on N-substrate wafers with different epitaxial layers.

For frequency response measurements on a wafer prober, the output signal of the OEICs was fed via a picoprobe into the network analyzer. Figure 12.21 shows the frequency response of the monolithic OEICs on a standard and on a low doped epitaxial layer and of the “wire-bonded” OEIC. The −3 dB bandwidth of the OEIC with the standard epitaxial layer with a doping concentration of approximately 1 × 10^{15} cm\(^{-3}\) is approximately 10 MHz. The best results are achieved with a low doping concentration (i.e., 5 × 10^{13} cm\(^{-3}\)) in the epitaxial layer (\(f_{3\,dB} = 19\) MHz). The “wire-bonded” OEIC on the same low doped epitaxial material has a much poorer performance (\(f_{3\,dB} = 4\) MHz).

For the packaged 8-channel DVD-OEIC with a total power consumption of approximately 70 mW, the following results were obtained: the offset voltage was smaller than 10 mV and the sensitivity of the fast channels was 3.3 mV µW\(^{-1}\). A value of 5.6 mV µW\(^{-1}\) was achieved with a special antireflection coating layer. The −3 dB bandwidth was measured with an active probe.

![Figure 12.21. Comparison of measured frequency responses for three different CMOS OEICs [95]](image)
head, whereby the amplifiers were loaded with $C_L = 11.2 \text{pF}$ and $R_L = 1 \text{k}\Omega$. Figures 12.22 and 12.23 show the frequency responses of a fast channel and of a slow channel with a ten times larger sensitivity, respectively.

For a fast channel, the $-3 \text{dB}$ bandwidth was $\approx 33 \text{MHz}$ for the high gain, $\approx 50 \text{MHz}$ for the medium gain, and $\approx 54 \text{MHz}$ for the low gain. These values far exceed the bandwidth of $7.3 \text{MHz}$ of the circuit for $8 \times$ speed CD-ROM, which was fabricated in a $0.8 \mu\text{m}$ CMOS technology and which used off-chip photodiodes [605]. The noise level at $10 \text{MHz}$ with a resolution bandwidth (RBW) of $30 \text{kHz}$ was $-89 \text{dBm}$. The group delay was constant within $\pm 2.5 \text{ns}$ for frequencies up to approximately $15 \text{MHz}$. For a slow channel, the $-3 \text{dB}$ bandwidth was $\approx 2.2 \text{MHz}$ for the high gain, $\approx 4.8 \text{MHz}$ for the medium gain, and $\approx 9.0 \text{MHz}$ for the low gain.
Let us summarize. For the standard doping level of the epitaxial layer, the first result is the 2.5 times larger bandwidth of the fully integrated circuit compared with the wire-bonded circuit. This enhanced performance is due to the minimized parasitic capacitances between the photodiodes and the amplifiers. The second result is that the performance of the PIN CMOS OEICs is enhanced when they are integrated on substrates with an epitaxial layer, which has a low doping concentration (e.g., $5 \times 10^{13}$ cm$^{-3}$). The depletion layer width of the PIN photodiode, which is reverse-biased, is greater in the case of the epitaxial material with $5 \times 10^{13}$ cm$^{-3}$ than in the case of the standard material. For a doping level of $5 \times 10^{13}$ cm$^{-3}$ in the epitaxial layer, the depletion layer reaches through the whole intrinsic region, and the slow diffusion of photogenerated carriers is eliminated. This results in a faster frequency response of the photodiode. With the results achieved, double-speed DVD video systems with PIN CMOS OEICs are possible.

### 12.4.4 BiCMOS Circuits for Optical Storage Systems

For optical storage (OS) systems with an enhanced data rate, BiCMOS OEICs were developed within the BiCMOS project. These OEICs contain four fast channels (A–D) for data extraction and focus control plus four slower channels (E–H) for tracking control with a ten times larger sensitivity (Fig. 12.24).

No process modifications were necessary in the BiCMOS process implementing a double photodiode shown in Fig. 3.112 [289]. The schematic of one

![Fig. 12.24. Block diagram of an OS-BiCMOS-OEIC](image)
fast channel of an eight-channel OS-BiCMOS-OEIC is shown in Fig. 12.25 [289]. Polysilicon-polysilicon capacitors are available in the 0.8 µm BiCMOS process and a transimpedance amplifier is realized here. The gain is switchable between high (H), medium (M), and low (L). Only NPN transistors are used in the signal path and the resistor loads R1 and R2 are implemented in the difference amplifier to achieve a high $\sim 3$ dB bandwidth. The value of 44 MHz was confirmed by measurements for the high gain [290]. The emitter follower Q5 reduces the output impedance of the operational amplifier.

The base currents of Q1 and Q2 in the input stage of the operational amplifier, flowing through the transimpedance resistor R3, leads to a systematic output offset voltage of approximately 0.1 V, when no special measures are taken. These special measures are the following: The transistors Q3 and Q4 are used to sense the base currents of Q1 and Q2, respectively. The current mirrors M1/M2 and M3/M4 mirror the base currents of Q3 and Q4 into the bases of Q1 and Q2, respectively [606]. With this bias current cancellation, the output offset voltage could be reduced to less than 9 mV [289].

The frequency responses for the three different gain factors of the OS-BiCMOS-OEIC are shown in Fig. 12.26. The $\sim 3$ dB bandwidth for the high gain is 44 MHz, for the medium gain it is 59 MHz, and for the low gain it is 64 MHz. The slightly decreasing frequency responses between 1 MHz and 40 MHz are due to parasitic capacitors in the amplifier and not due to slow carrier diffusion of photogenerated carriers in the double photodiode (DPD). The power consumption of the circuit in Fig. 12.25 is 7 mW at 5.0 V and with an antireflection coating a sensitivity of 10.5 mV µW$^{-1}$ is achieved with the highest gain factor. The active die area of this circuit is 0.054 mm$^2$. An 8-channel OEIC with four of the above described fast amplifiers and four ten times more sensitive MOS amplifiers consumed a power of approximately 40 mW.

Fig. 12.25. The fast channels A–D in an OS-BiCMOS-OEIC [289]
Fig. 12.26. Frequency response of a BiCMOS OEIC for optical storage systems for three different optical input powers, i.e., three different gain factors [289].

Fig. 12.27. Frequency responses of the fast channels A–D of a high-bandwidth BiCMOS OEIC for optical storage systems measured with three different optical input powers, i.e., three different gain factors [292].

At the expense of a higher power consumption, an even higher speed of OEICs for optical storage systems is possible [292]. A high-bandwidth BiCMOS OEIC has been demonstrated, which implemented fast amplifiers with the same schematic shown in Fig. 12.25 but with larger bias currents than in [289]. These fast amplifiers exhibit $-3\,\text{dB}$ bandwidths in excess of 90 MHz (Fig. 12.27).

An integrated double photodiode (Fig. 12.25) is connected to a transimpedance amplifier using an operational amplifier in order to obtain a low output offset voltage compared with a reference voltage of 2.5 V as is required for applications in optical storage systems. For a universal applicability, the
gain is switchable by MOS elements between high (H, R3), medium (M, R4 \parallel R3), and low (L, R5 \parallel R4 \parallel R3) with a ratio of approximately 1/3 each. Polysilicon-polysilicon capacitors are used for frequency compensation with C1, C2, and C3. Here, the bias current cancelation of the input transistors Q1 and Q2 reduces the systematic output offset of approximately 110 mV, which would result from the base current of Q1 across the resistor R3 \approx 20 \text{k}\Omega, to below 11 mV. According to simulations, the low-frequency open-loop gain of the operational amplifier is 27 dB, and its transit frequency is 870 MHz in the case of a load of 1 k\Omega and 10 pF. An OEIC was packaged, mounted together with these load elements on a printed circuit board, and the frequency responses were measured with a probe head having an input capacitance of 1.7 pF. The slight decrease in the frequency responses (Fig. 12.27) between about 5 and 80 MHz is due to parasitic capacitors in the amplifier and is not due to the slow diffusion of photogenerated carriers in the DPD. The measured bandwidths exceed a value of 92 MHz. This value is much larger than the bandwidth of 7.3 MHz of the circuit for 8\times speed CD-ROMs fabricated in 0.8 \mu m CMOS technology with off-chip photodiodes [605].

Figure 12.28 shows the schematic of the four sensitive channels E–H with a ten times larger sensitivity for tracking control in the optical storage system. A double photodiode with approximately twice the size of the DPDs in the channels A–D is implemented in the channels E–H. The N-channel MOSFET source followers M1 and M2 are added in front of the bipolar difference amplifier Q1 and Q2 in order to avoid input currents and the resulting output offset voltages across the feedback resistors of about 200 k\Omega. A high sensitivity of 100 mV \mu W\textsuperscript{-1} in combination with a low offset voltage can be realized in such a way. The PMOS load elements M3 and M4 are implemented for Q1 and Q2 in the difference amplifier in order to achieve a larger open-loop gain

\[ \text{Fig. 12.28. The sensitive channels E–H in a high-bandwidth OS-BiCMOS-OEIC} \]
than with resistor load elements. The compensation is split between C1 and C2, C1 and C3, as well as C1 and C4. According to circuit simulations, the low-frequency open-loop gain of the circuit shown in Fig. 12.28 is 36 dB with a transit frequency of 130 MHz.

The frequency responses of the channels E–H are shown in Fig. 12.29. The values for the −3 dB bandwidths are listed in Table 12.1 together with other results.

Each amplifier in the channels A–H covers an active die area of about 0.079 mm$^2$, and the total die area of the high-bandwidth BiCMOS OEIC amounts to 3.25 mm$^2$. The power consumption of the high-bandwidth OS-BiCMOS-OEIC is less than 75 mW at 5.0 V. Table 12.1 summarizes further technical data of the fast and the sensitive channels of the high-bandwidth OS-BiCMOS-OEIC.

Figure 12.30 shows the microphotograph of the OS-BiCMOS-OEIC with bandwidths in excess of 90 MHz, which was realized in full custom design. The results demonstrate that it is possible to avoid the slow carrier diffusion problem by exploiting double photodiodes in standard BiCMOS technology.

When a high speed and a higher sensitivity are required in addition to a low output offset voltage for the OS-OEICs, a two-stage optical receiver may be necessary. The circuit principle of such a two-stage amplifier [607] is shown in Fig. 12.31. The circuit consists of a transimpedance amplifier for the photocurrent and a reference I/U converter for offset compensation plus an operational amplifier in subtractor configuration. The subtractor can be used simultaneously as a voltage amplifier with the amplification factor $RS_2/RS_1$ enabling a high overall sensitivity of the OEIC. It must be mentioned,

![Figure 12.29](image)

**Fig. 12.29.** Frequency responses of the sensitive channels E–H of a high-bandwidth BiCMOS OEIC for optical storage systems measured with three different optical input powers, i.e., three different gain factors
Table 12.1. Measured results of the high-bandwidth OS-BiCMOS-OEIC

<table>
<thead>
<tr>
<th></th>
<th>H</th>
<th>M</th>
<th>L</th>
</tr>
</thead>
<tbody>
<tr>
<td>( f_{-3 , dB} ) (MHz) A–D</td>
<td>92.0</td>
<td>94.9</td>
<td>95.1</td>
</tr>
<tr>
<td>( f_{-3 , dB} ) (MHz) E–H</td>
<td>5.2</td>
<td>8.5</td>
<td>14.6</td>
</tr>
<tr>
<td>Sensitivity (mV ( \mu )W(^{-1} )) A–D</td>
<td>8.8</td>
<td>2.9</td>
<td>0.9</td>
</tr>
<tr>
<td>Sensitivity (mV/( \mu )W(^{-1} )) E–H</td>
<td>88.1</td>
<td>29.3</td>
<td>9.1</td>
</tr>
<tr>
<td>( U_{\text{Offset}} ) (mV) A–D</td>
<td>&lt;10.8</td>
<td>&lt;9.5</td>
<td>&lt;9.0</td>
</tr>
<tr>
<td>( U_{\text{Offset}} ) (mV) E–H</td>
<td>&lt;7.4</td>
<td>&lt;6.4</td>
<td>&lt;6.4</td>
</tr>
<tr>
<td>Noise (dB m) @10 MHz with 30 kHz RBW A–D</td>
<td>-81.5</td>
<td>-85.0</td>
<td>-85.2</td>
</tr>
<tr>
<td>Noise (dB m) E–H</td>
<td>-66.0</td>
<td>-67.5</td>
<td>-73.5</td>
</tr>
</tbody>
</table>

Fig. 12.30. Micrograph of a high-bandwidth BiCMOS DVD OEIC [292]

however, that offset voltages due to mismatch of the two transimpedance input amplifiers and due to mismatch in the operational amplifier are also amplified.
The circuit diagram of the complete circuit is shown in Fig. 12.32. In order to achieve a high bandwidth, only NPN transistors are used in the signal paths of the preamplifiers. Q1 is used in common-emitter configuration, Q3 is used as emitter follower, and the feedback resistor $R_{fb1}$ together with Q1 and Q3 represent a low input impedance for the photocurrent of the double photodiode (DPD). Thereby, the effect of the DPD capacitance is minimized. The reference voltage $V_{ref}$ is chosen as the emitter potential of Q1 to increase the reverse voltage of the DPD to $V_{BE,Q1} + V_{ref}$. The values for $R_1$, $R_{fb1}$, and $C_{fb1}$ were 3 kΩ, 27 kΩ, and 25 fF, respectively. A second emitter follower (Q11) is implemented for level shifting and decoupling of output and feedback.
path. The second preamplifier consists of transistors Q2, Q4, and Q12 as well as the current mirror with Q6 and Q7 and the feedback resistor $R_{fb2}$ plus the compensation capacitor $C_{fb2}$. At the outputs of the preamplifiers, C3 and C4 are added as further compensation capacitors.

The large signal DC transfer functions of the preamplifiers are given by

$$V_{pre1} = V_{ref} + \eta_{tia} I_{ph} R_{fb1} + I_{B,Q1} R_{fb1},$$

and

$$V_{pre2} = V_{ref} + I_{B,Q2} R_{fb2},$$

when we assume $U_{BE,Q1} = U_{BE,Q11}$ and $U_{BE,Q2} = U_{BE,Q12}$. The efficiency factor $\eta_{tia}$ of the preamplifier is given by $\eta_{tia} = R_1 \beta / (R_{fb1} + R_1 \beta)$. For $\beta = 100$ and for the resistor values given above the efficiency factor $\eta_{tia}$ of the transimpedance preamplifier is equal to 0.917. The base current of Q1 (and Q2) causes a voltage of about 0.1 V across $R_{fb1}$ (and $R_{fb2}$). In order to achieve a low output offset voltage compared with $V_{ref}$, therefore, the second preamplifier without a photodiode and the subtractor operational amplifier are necessary. Perfect matching of the two preamplifiers ($I_{B,Q1} = I_{B,Q2}$, $R_{fb1} = R_{fb2}$, $R_1 = R_2$, $\beta_1 = \beta_2$, $U_{BE,Q3} = U_{BE,Q4}$, $U_{BE,Q11} = U_{BE,Q12}$) is, however, necessary in order to obtain $V_{pre1} = V_{pre2}$ for a dark photodiode. This perfect matching of the two preamplifiers requires a careful layout to achieve a low output offset voltage.

The preamplifiers are connected to the subtractor operational amplifier via R5 and R6. The bias current cancelation introduced in Fig. 12.25 is applied to reduce the input currents of the operational amplifier necessary for a low output offset voltage. A PMOS current mirror load with M5 and M6 is used here in order to obtain a higher open loop gain of the operational amplifier. For $R_5 = R_6$ and $R_7 = R_8$, an analysis of the subtractor amplifier yields the transfer function

$$V_{out} = V_{ref} + \frac{R_7 A_d(s)}{(R_6 + R_7) + R_6 A_d(s)} (V_{pre1} - V_{pre2})$$

and

$$V_{out} \approx V_{ref} + \frac{R_7}{R_6} \eta_{tia} I_{ph} R_{fb1},$$

when we assume a large open loop voltage gain $A_d(s)$ of the operational amplifier. A $-3$ dB frequency of 189 MHz was determined by numerical prelay-out simulation for the complete amplifier with a load of $R_L = 1 \text{k}\Omega$ and $C_L = 10 \text{pF}$. The complete two-stage preamplifier was designed for a sensitivity of 10 mV $\mu$W$^{-1}$ and an offset voltage of less than 10 mV for $R_5 = R_6 = R_7 = R_8$.

The OEIC with the DPD and the two-stage amplifier was fabricated in a 0.8 $\mu$m BiCMOS technology. The measured frequency response of this two-stage optical receiver is shown in Fig. 12.33. A $-3$ dB frequency of 147.7 MHz is determined from this frequency response. The power consumption of the two-stage optical receiver is 35 mW at a supply voltage of 5 V. The active die area of the two-stage optical receiver is $340 \times 140 \mu$m$^2$. 
12.4.5 Fiber Receivers

Optical multimode fibers for optical data transmission usually possess a core diameter of 50 or 62.5 µm. The core diameter of single-mode fibers for wavelengths shorter than 1.1 µm is actually less than 10 µm. Small-area photodiodes, therefore, can be used in order to realize a low capacitance at the input of the receiver circuits. The bondpad capacitances of wire-bonded receivers are much larger than the capacitance of PIN photodiodes. Monolithically integrated optical fiber receivers should be the first choice as a consequence. In the following, a bipolar OEIC, two NMOS OEIC, two BiCMOS OEICs, and several CMOS OEICs for the application as fiber receivers will be described.

Bipolar SiGe Receiver

The superior speed of SiGe HBTs compared with Si bipolar transistors has already been mentioned and the structure of a monolithic SiGe–Si PIN-HBT receiver was described in Chap. 6. Here, the bipolar transimpedance amplifier circuit of this receiver (see Fig. 12.34) will be discussed.

The receiver consists of a PIN photodiode, a common emitter gain stage, two emitter follower buffers, and a resistive feedback loop. NiCr thin-film resistors were used in the monolithic SiGe HBT receiver [404]. The transistors Q1, Q4, and Q5 are used as level shifting diodes. Q1 and Q5 reduce $U_{CE}$ of Q2 and Q6, respectively, because the breakdown voltages of high-speed transistors are quite low.

The two voltage sources VDD and VCC were necessary to optimize the PIN transient behavior and the operating point of the amplifier. The value of the feedback resistor $R_F$ determines the bandwidth, gain, and noise characteristics of the photoreceiver. The value of $R_F$ is usually chosen based on a trade-off
between these three parameters. In [404], a value of 640 Ω was chosen for $R_F$ resulting in a transimpedance gain of 52.2 dB Ω. The bandwidth of 1.6 GHz was obtained for the transimpedance amplifier with a $f_T$ of 25 GHz for the HBTs with an emitter area of $5 \times 5 \mu m$. The optical bandwidth of 460 MHz of the PIN-HBT receiver was measured for VDD = 9 V and VCC = 6 V. The bandwidth of the receiver was limited by the photodiode, and the trade-off mentioned above might be improved with respect to an increased gain, i.e., a larger sensitivity. An input noise spectral density of 8.2 pA per $\sqrt{Hz}$ up to 1 GHz caused by shot noise from the base current and thermal noise from the feedback resistor was given. With these values, the photoreceiver sensitivities of $-24.3$ and $-22.8$ dB m were estimated for 0.5 and 1 Gb s$^{-1}$, respectively, for a bit error rate (BER) of $10^{-9}$ and $\lambda = 850$ nm.

NMOS Receivers

The next example is an NMOS OEIC. A lateral PIN photodiode was integrated in a 1.0 µm NMOS technology using a nominally undoped substrate, which was actually P-type with $N_A = 6 \times 10^{12}$ cm$^{-3}$ [85,86]. This lateral PIN photodiode is described in Sect. 3.5.3.

An NMOS transimpedance preamplifier (Fig. 12.35) implementing a depletion transistor at the input was integrated together with a lateral PIN photodiode (see Fig. 3.21). The second and third stages were formed by source followers. The source follower stage M3/M4 with M4 as a constant current source is used to establish the correct operating point across the feedback loop with MF as an active resistor. The source follower stage M5/M6 at the
output was sized to match a 50 Ω load impedance. The power dissipation including the output driver was only 3 mW. Accordingly, open-eye operation for bit-rates of only up to 40 Mb s\(^{-1}\) with a photocurrent of 3 μA for \(\lambda = 870\text{nm}\) and for a transimpedance of 3 kΩ was reported [85].

The authors of [85], meanwhile, improved their photoreceiver [608]. An N-type Si substrate with a resistivity of 1,000–3,000 Ω cm was taken and an interdigitated lateral PIN structure with a finger width of 2 μm and a finger spacing of 10 μm instead of the ring structure (see Fig. 3.21) was implemented. The total area of the photodiode was 50 × 50 μm\(^2\). A dark current of 1.3 pA at 5 V and of 63 nA at 30 V was found. The quantum efficiency was increased to 84 and 74% at 800 and 870 nm, respectively, due to an SiO\(_2\) antireflection coating with a thickness of 150 nm. A bit-rate of 500 Mb s\(^{-1}\) was achieved from the interdigitated PIN photodiode at 30 V; however, its frequency response showed a diffusion tail below 100 MHz [608].

The preamplifier has also been modified. Figure 12.36 shows the improved three-stage preamplifier. The feedback via M3 is only across the first stage with the common-source amplifier M1 and the depletion load M2. The second stage with the enhancement mode MOSFETs M4 and M5 further amplifies the signal and is used as a buffer to drive the depletion source follower M7 with an output impedance of 50 Ω. At the optimum feedback, \(V_F = 1.25\) V, the transimpedance was 6.5 kΩ and a 45 μA dynamic range of the photocurrent was obtained. The bandwidth of the photoreceiver was 130 MHz for 870 nm light, when biased with VDD = 8 V, \(V_F = 1.25\) V, and \(V_{PIN} = 30\) V. Open-eye operation under these conditions was demonstrated up to 300 Mb s\(^{-1}\). The sensitivity of the photoreceiver was \(-33\) dB m at 155 Mb s\(^{-1}\) and \(-25.5\) dB m at 300 Mb s\(^{-1}\) at a bit error rate (BER) of \(10^{-9}\) for a pseudo-random bit sequence (PRBS) of \(2^{23} - 1\) under the same conditions. At a bias of VDD = 8 V,
the power dissipation was 44 mW, with 2 mW from the first two stages. A redesigned circuit \cite{609} achieved sensitivities of $-22.8$, $-15$, and $-9.3$ dBm at bit rates of 622, 900, and 1,000 Mb s$^{-1}$, respectively. This redesigned preamplifier had a bandwidth of 500 MHz and dissipated only 10.8 mW at a power supply voltage of 1.8 V. $V_{\text{PIN}} = 30$ V, however, was still necessary for a $-3$ dB frequency of 150 MHz and a $-6$ dB frequency of about 750 MHz for the lateral PIN photodiode.

It can be concluded that the approach of \cite{608,609} results in a rather good performance of the photoreceiver at the cost, however, of a rather large supply voltage of 30 V for the lateral PIN photodiode. This voltage is usually not present in modern electronic systems and advanced microelectronic circuits, which operate at 5, 3.3, 2.5, 1.8 V or even lower voltages.

**BiCMOS Receivers**

Results of BiCMOS-OEICs, consisting of a PIN photodiode and an amplifier, which exploited only MOSFETs and no bipolar transistors, have been published \cite{287,288}. The BiCMOS technology, therefore, was chosen merely for the integration of the PIN photodiode. A standard BiCMOS technology with a minimum effective channel length of 0.45 $\mu$m was used without any modifications \cite{287,288}. This effective channel length corresponds to a drawn or nominal channel length of about 0.6 $\mu$m. The buried $N^+$ collector in Fig. 3.109 was used for the cathode of the PIN photodiode, the $P^+$-source/drain island served for the anode, and the intrinsic zone of the PIN photodiode was formed by the N well (see Sect. 3.7).

The circuit diagram of the CMOS preamplifier used in the BiCMOS OEIC is shown in Fig. 12.37. The input stage of this amplifier with the NMOS transistors $N_1$, $N_2$, and $N_3$ is a single-ended transimpedance amplifier featuring DC input coupling. The feedback resistor $R_3$ had a value of 1.4 k$\Omega$. However,
with the additional voltage gain of the following circuit elements, the effective transimpedance of the amplifier was about 3.0 kΩ. The circuit with the transistors N5 and N6 produces a reference voltage at the gate of P5. This voltage is close to the midpoint of the voltage swing at the gate of P3 and can be considered as a kind of decision threshold. P3 and P5 are source followers, which are biased by the current sources P2 and P4, respectively. N4–N6 and P1–P5 perform a single-ended to differential conversion. N7 and N8 form a differential amplifier. N10–N13 are source-follower drivers with an output impedance of 50Ω.

The power dissipation of the core amplifier circuit was 30 mW from a 3.3 V supply, with an additional 57 mW in the output source followers. The −3 dB bandwidth of the receiver was 300 MHz. The OEIC reached a bit rate of 531 Mb s⁻¹ with a bit error rate of 10⁻⁹ and a sensitivity of −14.8 dBm for λ = 850 nm.

In [288] a laser with a wavelength of 670 nm was used for the characterization of the same OEIC as in [287]. The data rate was increased to 622 Mb s⁻¹ for this wavelength. This bit rate was limited by the capacitance of the photodiode and the feedback resistor of 1.4 kΩ in the amplifier transimpedance input stage.

Another BiCMOS fiber receiver OEIC has been described containing a double photodiode (Fig. 3.112) and a bipolar preamplifier (Fig. 12.38). This OEIC has been fabricated in a 0.8 µm BiCMOS technology.

The transistor Q1 is used in common-emitter configuration. Together with the emitter follower Q2 and the feedback resistor R_fb, Q1 forms a transimpedance input stage. The emitter follower Q4 is used for level shifting and for decoupling the feedback loop from the output. A reference voltage V_REF of 2.5 V has been applied to the emitter of Q1 resulting in a reverse bias of about 3.3 V for the double photodiode lying between the input and ground.
Fig. 12.38. Fiber receiver OEIC fabricated in BiCMOS technology [610]

Fig. 12.39. Eye diagram of a BiCMOS fiber receiver OEIC recorded at 531 Mbs$^{-1}$ with a PRBS word length of $2^{23} - 1$ (time scale: 400 ps per div; amplitude: 100 mV per div) [610]

The transient response of a double photodiode with an area of $530 \mu m^2$ shown in Fig. 3.116 has been measured with this amplifier. A bandwidth of 367 MHz has been determined for the OEIC. Wide-open eye patterns with a turn-on delay of 0.2 ns at a bit rate of 531 Mbs$^{-1}$ for $\lambda = 638$ nm (Fig. 12.39) were obtained with this BiCMOS OEIC containing a double photodiode with an area of $530 \mu m^2$ in a standard technology without any modifications [610].

CMOS Receivers

Another field of application for OEICs in addition to fiber receivers is optical interconnect technology, because electrical interconnects on a board or system level are becoming a problem due to steadily increasing clock frequencies. In particular, signal reflections on long interconnects, on large boards, and the cross talk on high-density electronic boards with conductor widths of 0.1 mm
and conductor spacings of 0.1 mm are critical. Optical interconnects, e.g., via waveguide-in-board or fiber-in-board and optical backplanes, avoid the problems of electrical interconnects.

For the application in optical interconnect technology, a CMOS preamplifier OEIC was developed choosing the innovative monolithic integration of vertical PIN photodiodes in a twin-well CMOS-process (Fig. 3.36) [89], which uses epitaxial wafers. The integration of PIN photodiodes in such a CMOS technology requires much less additional process complexity than the published approaches to standard-buried-collector (SBC) based bipolar OEICs [38, 59]. Three additional masks were necessary for the PIN-bipolar integration and for the avoidance of the Kirk effect [38]. Only one photodiode protection mask is added for the PIN-CMOS integration in order to block out an originally unmasked threshold implantation from the photodiode area. A reduction of the standard doping concentration $C_e$ of approximately $1 \times 10^{15}$ cm$^{-3}$ in the epitaxial layer was necessary in order to obtain fast integrated PIN photodiodes. In contrast to a reduction of the current gain and of the transit frequency of bipolar transistors in bipolar OEICs due to the Kirk effect, the electrical performance of the N- and P-channel MOSFETs is not degraded when the doping level in the epitaxial layer is reduced, because these MOSFETs are placed in wells [89]. Reach-through and electrostatic discharge (ESD) aspects in the CMOS OEICs can be dealt with using appropriate design measures.

In contrast to the OEIC of [608], here, only a single power supply of 5 V is needed. The circuit of the preamplifier OEIC is shown in Fig. 12.40.

The amplifier consists of three stages. The input stage with M1–M3 is a transimpedance configuration. The source followers M2, M5, and M8 as well as the current sources M3, M6, and M9 are used for level shifting. Without these transistors, $V_{GS}$ of transistor M1 would be larger, and a lower voltage across the PIN photodiode would result and would increase the rise and fall

![Circuit diagram](image)

**Fig. 12.40.** Circuit diagram of a CMOS preamplifier OEIC [92]
times of its photocurrent. The threshold implant in Fig. 3.22g was omitted to reduce the threshold voltage of transistors M2, M5, and M8 intentionally to about 0.4 V by using the photodiode protection mask to obtain lower $V_{GS}$ values and to realize the optimum level shifting in such a way. Because of the feedback across the 2.2 kΩ transimpedance resistor and the identical dimensions of the transistors in the different stages, a good independence from process deviations within the relatively large specified process tolerances of the used digital CMOS process is obtained.

The CMOS receiver OEIC was fabricated in a 1.0 µm industrial CMOS process [93]. The microphotograph of the CMOS preamplifier OEIC can be seen in Fig. 12.41.

The photodiode, having a light sensitive area of 2,700 µm$^2$, together with its metal shield around covers an area of approximately 150 × 150 µm$^2$. The preamplifier occupies an active area of less than 130 × 200 µm$^2$. The sensitivity of the PIN CMOS preamplifier OEIC was 4.7 mV µW$^{-1}$ without ARC, and its power consumption was 19 mW at 5.0 V.

The oscilloscope extracted a rise time $t_{osc,\, disp} = 15.5$ ns and a fall time $t_{f,\, disp} = 17.6$ ns for the OEIC with the doping concentration of $1 \times 10^{15}$ cm$^{-3}$ in the epitaxial layer for a laser wavelength of 638.3 nm. These large values for $t_r$ and $t_f$ are due to the slow carrier diffusion in the standard epitaxial layer of the photodiode. The corresponding values for the concentration of $2 \times 10^{13}$ cm$^{-3}$ in the epitaxial layer, where the depletion region spreads through the whole epitaxial layer and carrier diffusion in the photodiode is eliminated, were 1.05 and 1.26 ns, respectively [92].

Figure 12.42 shows the eye diagram of the CMOS preamplifier OEIC in Figs. 12.40 and 12.41. The eye diagram was measured on the wafer level with a picoprobe (input capacitance: 0.1 pF) at the output of the OEIC, with an HP54750/51 digital sampling oscilloscope, and with an ECL bit pattern generator, which modulated a red semiconductor laser with a wavelength of

![Fig. 12.41. Microphotograph of a CMOS receiver OEIC [92]](image-url)
Fig. 12.42. Measured eye diagram of a CMOS preamplifier OEIC for the application in a fiber and interconnect receiver (time: 500 ps per div, amplitude: 0.2 V per div) [92]

Fig. 12.43. CMOS inverter receiver OEIC [76]

638.3 nm. A pseudo-random bit sequence (PRBS) of $2^{23} - 1$ in a non-return-to-zero (NRZ) bit rate of 320 Mb s$^{-1}$ was used. The doping concentration in the epitaxial layer of the wafer which was used for the fabrication of the OEIC was $2 \times 10^{13}$ cm$^{-3}$.

Simulations showed that shorter rise and fall times can be expected for an improved preamplifier and bit rates in excess of 600 Mb s$^{-1}$ seem feasible for a wavelength of 638 nm. For wavelengths of 780 and 850 nm, bit rates of 500 Mb s$^{-1}$ were estimated by simulations [92]. Meanwhile, the OEIC has been characterized by eye diagram measurements at a bit rate of 622 Mb s$^{-1}$ with a wavelength of 638 nm [97].

The fast fully integrated single-beam optical bulk CMOS receiver (Fig. 12.43) was realized in the Lucent 0.35 μm production process [76]. This receiver contained the photodetector shown in Fig. 3.17. The amplifier of this receiver is formed by three inverter stages. The first stage with the inverter M1 and M2 is a transimpedance stage with the P-channel MOSFET
M8 as the feedback element. The gate voltage of M8 could be adjusted for optimum performance ($V_{\text{tune}}$) at a given optical power and bit rate. This first stage converts the photocurrent, flowing from the anode of the photodiode through the active resistor M8, into a voltage. The second stage with the inverter M3, M4 amplifies this voltage. The N-channel MOSFET load M5 reduces the gain and increases the bandwidth. With M5, the technology dependence of the amplifier gain is reduced and the switching threshold of this stage is stabilized [611]. The third stage with M6 and M7 supplies a high gain. This stage acts as an asynchronous decision circuit resulting in a fully digital logic output level. For a correct and optimum performance of this DC-coupled three-stage preamplifier circuit, the dimensions of the transistors M5 and M8 have to be chosen carefully [76].

The supply voltage of the preamplifier was varied between 1.8 and 3.3 V. The best sensitivity was obtained at a supply bias of $V_{\text{DD}} = 2.2$ V. A bit error rate of $10^{-9}$ for a bit rate of $1 \text{ Gb s}^{-1}$ was obtained with an average optical input power of $-6.3 \text{ dB m}$ and with a detector bias $V_{\text{det}} = 10$ V. This low sensitivity results from the low responsivity of the photodiode of less than $0.04 \text{ A W}^{-1}$. Another disadvantage of this OEIC is the high detector bias of 10 V.

For an OEIC fabricated in a 0.25 $\mu$m fully-depleted CMOS SOI process technology, a single 2 V supply was sufficient [311]. The photodetector of this OEIC was a lateral PIN photodiode exploiting the avalanche effect to achieve a high responsivity of $0.4 \text{ A W}^{-1}$, although the OEIC was fabricated in a very thin SOI layer (see Fig. 4.8). The amplifier circuit of this OEIC is shown in Fig. 12.44.

The preamplifier circuit is based on a transimpedance amplifier with a feedback resistor $R_{\text{fb}}$ of 5 kΩ. The N-channel MOSFET N1 is used in a common-source circuit. The PMOS transistor P1 forms the active load for N1. N2 is used as source follower to obtain a low output impedance of the transimpedance input stage. N3 is a constant-current source. N4 am-

![Fig. 12.44. CMOS receiver OEIC on SOI [311]](image-url)
Examples of Optoelectronic Integrated Circuits

Plifies the output voltage of the transimpedance input stage. P6 is used as a source follower for shifting the signal level toward VDD and reducing the output impedance. This shifting toward VDD is necessary to allow the implementation of the second source follower N7 for further reducing the output impedance. P5 and N8 are constant-current sources. P3, P4, N5, and N6 supply the reference voltage $V_{\text{ref}}$ for biasing the amplifier. The constant-current sources P1, P2, and P5 are set by P3. These four transistors form current mirrors.

Using a 850 nm wavelength, a bandwidth of 1 GHz was measured for a supply voltage of 2 V for an average optical input power of $-13$ dBm (50 µW) [311]. The OEIC occupied an area of $650 \times 400 \mu m^2$.

On the basis of the circuit shown in Fig. 12.40, an improved CMOS photoreceiver (Fig. 12.45), which contains a vertical PIN photodiode and which combines a data rate of 622 Mb s$^{-1}$ with a quantum efficiency of 94%, has been developed here. The innovative monolithic integration of vertical PIN photodiodes in a twin-well CMOS process (Fig. 3.36) [89] which uses epitaxial wafers, has been demonstrated to combine both high speed and large quantum efficiency of the photodiode [92]. In contrast to the OEICs of [76, 608], only a single power supply of 3.3 V was needed. The circuit of the high-bandwidth preamplifier with an integrated PIN photodiode is shown in Fig. 12.45. It is a typical high-frequency amplifier. Only N-channel MOSFETs are used to obtain a high bandwidth. The input stage with the transistors M1–M4 is a transimpedance configuration, which converts the photocurrent change in the integrated PIN photodiode to a voltage change. The cascode transistors M1, M5, and M9 reduce the Miller effect and increase the bandwidth correspondingly. The source followers M3, M7, and M11 as well as the current sources M4, M6, and M8.

![Circuit diagram of a CMOS preamplifier OEIC with a possible data rate of 622 Mb s$^{-1}$ for application in a fiber and interconnect receiver](image)

Fig. 12.45. Circuit diagram of a CMOS preamplifier OEIC with a possible data rate of 622 Mb s$^{-1}$ for application in a fiber and interconnect receiver [92]
M8, and M12 are used for level shifting. The threshold voltage of transistors M3, M7, and M11 has been reduced intentionally to about 0.4 V by the photodiode protection mask to obtain lower \( V_{GS} \) values. Polysilicon resistors were employed as load elements, since depletion transistors were not available in the digital CMOS process. Because of the feedback across the 2 k\( \Omega \) resistor and to the identical dimensions of the transistors in the different stages, a good independence from process deviations within the relatively large specified process tolerances of the digital CMOS process used has been obtained. Three identical biasing circuits (UB1=UB2=UB3) are used instead of one to minimize parasitic coupling between the stages. The sensitivity of the PIN preamplifier OEIC was 4.7 mV \( \mu \)W\(^{-1} \) for \( \lambda = 638 \) nm increasing to 9.0 mV \( \mu \)W\(^{-1} \) with ARC, which corresponds to an overall transimpedance of 18.4 k\( \Omega \). Its power consumption was 44 mW at 5.0 V reducing to 17 mW at 3.3 V.

The photodiode, together with its metal shield around, covers an area of approximately 150 \( \times \) 150 \( \mu \)m\(^2\) (see Fig. 12.46). The preamplifier occupies an active area of less than 190 \( \times \) 200 \( \mu \)m\(^2\).

Values of 0.62 and 0.86 ns for the rise and fall times, respectively, at the output of the preamplifier (Fig. 12.47) were extracted by a digital sampling oscilloscope for a concentration of 2 \( \times \) 10\(^{13} \) cm\(^{-3} \) in the epitaxial layer, where the depletion region spreads through the whole epitaxial layer already with a supply voltage of 3.3 V.

The correction of the \( t_{r/f} \) values for the laser and picoprobe rise and fall times results in \( t_{r}^{OEIC} = 0.53 \) ns and \( t_{f}^{OEIC} = 0.69 \) ns. These values indicate that CMOS OEICs with a reduced doping concentration in the epitaxial layer having an appropriate output buffer can be used as receivers for optical data transmission via fibers or for optical interconnects on a board level up to a bit rate BR of 622 Mb s\(^{-1} \) in the non-return-to-zero (NRZ) mode, verified by a measured eye diagram with a pseudo-random bit sequence (PRBS) of 2\(^{23} \) − 1.

**Fig. 12.46.** Microphotograph of a high-speed CMOS receiver OEIC [96]
Fig. 12.47. Waveform at the output of the CMOS preamplifier OEIC with a possible data rate of 622 Mb s$^{-1}$ for application in a fiber and interconnect receiver

![Waveform at the output of the CMOS preamplifier OEIC](image1)

Fig. 12.48. Measured eye diagram of a CMOS preamplifier OEIC with a possible data rate of 622 Mb s$^{-1}$ for application in a fiber and interconnect receiver (time: 500 ps per div, amplitude: 0.1 V per div) [92]

(Fig. 12.48). The data rate of the OEIC has been limited by the amplifier in a 1.0 $\mu$m technology. With sub-micrometer PIN-CMOS-OEICs, however, data rates in excess of 1 Gb s$^{-1}$ are possible.

**Comparison**

It is worthwhile to compare published results on silicon OEICs in Table 12.2. A hybrid receiver-transmitter circuit consisting of a 0.8 $\mu$m CMOS amplifier and of a flip-chip bonded GaAs–AlGaAs multi-quantum-well modulator, which also could be used as a PIN photodiode, has been reported to operate at 625 Mb s$^{-1}$ [442]. A SiGe OEIC with a PIN photodiode and heterojunction...
### Table 12.2. Comparison of silicon receiver OEICs

<table>
<thead>
<tr>
<th>Process</th>
<th>VDD (V)</th>
<th>λ (nm)</th>
<th>BR&lt;sub&gt;PR&lt;/sub&gt; (Mbs⁻¹)</th>
<th>V&lt;sub&gt;PD&lt;/sub&gt; (V) or f&lt;sub&gt;3dB&lt;/sub&gt;</th>
<th>R&lt;sub&gt;PD&lt;/sub&gt; (A W⁻¹)</th>
<th>η&lt;sub&gt;PD&lt;/sub&gt; (%)</th>
</tr>
</thead>
<tbody>
<tr>
<td>0.8 CMOS-MQW</td>
<td>5</td>
<td>850</td>
<td>625</td>
<td>2.5</td>
<td>-</td>
<td>0.5</td>
</tr>
<tr>
<td>Bipolar SiGe</td>
<td>6</td>
<td>850</td>
<td>690</td>
<td>9</td>
<td>460 MHz</td>
<td>0.3&lt;sup&gt;a&lt;/sup&gt;</td>
</tr>
<tr>
<td>1.0 NMOS</td>
<td>8</td>
<td>870</td>
<td>300</td>
<td>30</td>
<td>500 Mb s⁻¹</td>
<td>0.52&lt;sup&gt;a&lt;/sup&gt;</td>
</tr>
<tr>
<td>Bipolar</td>
<td>5</td>
<td>850</td>
<td>1,000</td>
<td>30</td>
<td>1.0 Gb s⁻¹</td>
<td>0.54&lt;sup&gt;a&lt;/sup&gt;</td>
</tr>
<tr>
<td>Bipolar</td>
<td>5</td>
<td>780</td>
<td>50</td>
<td>3.0</td>
<td>300 MHz</td>
<td>0.35</td>
</tr>
<tr>
<td>Bipolar</td>
<td>5</td>
<td>830</td>
<td>150</td>
<td>3.0</td>
<td>280 MHz</td>
<td>0.5&lt;sup&gt;a&lt;/sup&gt;</td>
</tr>
<tr>
<td>0.6 BiCMOS</td>
<td>3.3</td>
<td>850</td>
<td>531</td>
<td>2.5</td>
<td>700 MHz</td>
<td>0.07</td>
</tr>
<tr>
<td>0.6 BiCMOS</td>
<td>3.3</td>
<td>670</td>
<td>622</td>
<td>2.5</td>
<td>700 MHz</td>
<td>0.16</td>
</tr>
<tr>
<td>0.8 BiCMOS</td>
<td>5</td>
<td>638</td>
<td>531</td>
<td>3.3</td>
<td>531 Mb s⁻¹</td>
<td>0.49</td>
</tr>
<tr>
<td>0.35 CMOS</td>
<td>3.3</td>
<td>850</td>
<td>1,000</td>
<td>10</td>
<td>1.0 Gb s⁻¹</td>
<td>0.04</td>
</tr>
<tr>
<td>0.25 CMOS SOI</td>
<td>2.0</td>
<td>850</td>
<td>1,500</td>
<td>1.5</td>
<td>1.0 GHz</td>
<td>0.4</td>
</tr>
<tr>
<td>1.0 CMOS</td>
<td>5</td>
<td>638</td>
<td>622</td>
<td>3.0</td>
<td>1.7 GHz</td>
<td>0.25</td>
</tr>
<tr>
<td>1.0 CMOS</td>
<td>3.3</td>
<td>638</td>
<td>622</td>
<td>1.8</td>
<td>1.4 GHz</td>
<td>0.48&lt;sup&gt;a&lt;/sup&gt;</td>
</tr>
</tbody>
</table>

<sup>a</sup>With ARC

bipolar transistors achieved a bandwidth of 460 MHz corresponding to a bit rate of about 690 Mbs⁻¹ with a photodiode bias of 9 V [404]. A lateral PIN photodiode was used in an NMOS receiver OEIC, which operated at a bit rate of 300 Mbs⁻¹ [608], when biased at VDD = 8 V and with a photodiode bias V<sub>PD</sub> = 30 V. In a redesigned version, the NMOS OEIC achieved a data rate of 1 Gb s⁻¹ at a sensitivity of −9.3 dB m [609].

With a bipolar OEIC [40] using the BEST-process of AT&T with 1.5 μm design rules [612], a data rate of 150 Mbs⁻¹ was achieved. An N<sup>+</sup>/P-substrate photodiode limited the speed to this data rate. In [38] and [59], vertical PIN photodiodes have been integrated with bipolar transistor technology. The optical receivers described in these two articles demonstrated a data rate of 50 Mbs⁻¹ [38] and a frequency response of 147 MHz [59] at a supply voltage of 5 V although the PIN photodiodes showed bandwidths of ≈300 MHz at a bias of 3 V. The thin P<sup>+</sup>/N-collector/N<sup>+</sup>-buried collector PIN photodiode in a 0.6 μm BiCMOS process was used together with a MOS amplifier in [287,288] with a rather low responsivity of the photodiode. A double photodiode in a standard 0.8 μm BiCMOS technology enabled a bit rate of the OEIC with a bipolar amplifier in excess of 531 Mbs⁻¹ [74,610]. A very low responsivity of 0.04 A W⁻¹ has been reported for the P<sup>+</sup>/N-well photodiode of a 1 Gb s⁻¹ OEIC in a 0.35 μm CMOS technology [76]. The most sophisticated avalanche photodiode approach in an SOI CMOS technology enabled an OEIC with a bandwidth of 1 GHz corresponding to a bit rate of about 1.5 Gb s⁻¹ at a supply voltage of only 2 V [311]. Summarizing, a low responsivity has been present to
achieve a high data rate in the investigations \[40,76,287,288\], or a high voltage for the photodiode was needed \[404,608,609\], or a high additional process complexity has been needed for the integration of fast and highly efficient photodiodes as in \[38,59\]. Even compared with the sophisticated detectors in \[76\] and \[311\], the vertically integrated PIN photodiode developed in the CMOS DVD project and described in \[92\] achieved the highest speed and the highest quantum efficiency with an antireflection coating. The CMOS-integrated vertical PIN photodiode, therefore, shows the largest speed-responsivity product of all integrated silicon photodiodes reported so far, whereby, standard or near-standard processes have been used.

It can be concluded that with CMOS receiver OEICs comparable or even better data rates can be obtained than with the bipolar OEICs described in \[38,59\]. In contrast to the integration of PIN photodiodes in bipolar circuits, the integration of vertical PIN photodiodes in CMOS circuits requires little additional process complexity. The vertical PIN photodiodes combine a high data rate and a high quantum efficiency at a low reverse bias with a single power supply voltage for the OEIC. Low cost PIN-CMOS receiver OEICs for optical data transmission and for optical interconnects on boards and between boards via optical backplanes seem feasible.

### 12.5 Summary

Digital optical CMOS receivers based on sense-amplifier flip-flops, which require small die areas and are therefore very interesting for the application in massively parallel optical interconnects, were described. OEICs with current mirror amplifiers and current comparators were shown to be appropriate for the wafer-level test of digital CMOS and BiCMOS circuits with considerably increased frequencies.

Many analog photoreceiver circuits were included in this chapter. For instance, a bipolar circuit for optical flame detection with a very high transimpedance and the pixel circuit of an amorphous-silicon-CMOS imager with a dynamical range of 100dB were described.

The most important results obtained so far within the two projects for the development of OEICs for optical storage systems are as following: PIN CMOS OEICs for DVD (video) applications with bandwidths in excess of 33 MHz were realized in full custom design. This bandwidth exceeds that of Japanese OEICs for twofold DVD speed \[613\]. A monolithic integrated CMOS OEIC was shown to exceed the bandwidth of a wire-bonded optoelectronic receiver circuit by a factor of 2.5 due to the avoidance of the bondpad capacitances. A monolithic integrated CMOS OEIC with a reduced doping concentration in the epitaxial layer increased the bandwidth by another factor of two.

The integrated PIN photodiodes can handle much higher data rates (>1 Gb s\(^{-1}\)) than are necessary for DVD applications. Therefore, a 1.0 µm PIN CMOS OEIC for fiber receiver applications with a non-return-to-zero
(NRZ) data rate of $622 \text{Mb s}^{-1}$ was demonstrated. This data rate was limited by the amplifier in 1.0 $\mu\text{m}$ CMOS technology. OEICs with data rates in excess of $1 \text{Gb s}^{-1}$, therefore, are possible with submicrometer CMOS processes. Possible applications for PIN CMOS OEICs are Local Area Networks (LANs), such as the Gigabit Ethernet or the Fiber Channel.

A BiCMOS full custom OPTO-ASIC for optical storage systems (CD-ROM, DVD-ROM, DVD-RAM) with bandwidths in excess of 90 MHz has been developed. This bandwidth exceeds that of Japanese OEICs for fourfold DVD speed [607] by almost a factor of two. Meanwhile, an even faster OEIC with a bandwidth of 147 MHz has been demonstrated within the projects for the development of OEICs for optical storage systems [293].